Survey of Current Correlators and Applications

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With larger scale integrated circuits becoming available, many new applications are becoming feasible for digital correlators. Numerous projects at JPL and elsewhere now have correlators included in systems. With this survey an attempt was made to contact as many users as possible so as to provide summary data on correlator systems, both in use and planned. Data on currently available VLSI chips and complete systems are included. Also, several planned correlator systems are described and summarized in tabular form. Finally, a description is given of the work being done in the Communications Systems Research Section (JPL Section 331) on VLSI correlator chips and complete correlator systems.

I. Introduction

Modern circuit techniques have permitted the design of much higher performance correlators than was possible a few years ago. Several groups at JPL and elsewhere are planning or already building new correlator systems. Typical areas of application for new correlators are radio and radar astronomy, long distance communications and deep space navigation. This survey was undertaken to determine the nature of the different correlation requirements for the various users with the goal being to examine and compare the different correlation requirements and determine what features they have in common. It was then to be determined if a multipurpose correlator machine might be designed. Also of interest was the structure that a hypothetical multipurpose correlator chip should have.

A brief overview of correlator hardware currently in use is given in Section II. First, the available off-the-shelf correlator chips are surveyed and second, a sample of correlator systems currently in use are described. Tables 1 and 2 summarize these results.

Information on correlators under development and projected future needs was collected from the various groups with correlator requirements. The results are displayed in summary form in Table 3 and are discussed more thoroughly in Section III. This survey is by no means exhaustive but gives a good overview of several typical applications for correlators.

A summary of work being done in the Communications Systems Research Section (Section 331) on VLSI correlator chips and systems is presented in Section IV. This is followed by some suggestions for architectures for implementing large high-performance correlator systems.

II. Devices and Systems Available

The following paragraphs represent a survey of some of the available correlator hardware. First, a description is given of the known VLSI correlator chips. At present there are four organizations known, outside of JPL, who produce VLSI correlator devices. Next, a sampling of correlator systems currently in use is discussed.

A brief definition of the correlation process will be useful for the ensuing discussions. Figure 1 illustrates a single lag cell of a complete correlator, that is, one containing multipliers, accumulators, and two data paths. The function of this ith lag cell is to perform the operation

$$C_i = \sum_{k=1}^{N} a_k b_{k+i}$$

where N is the duration of the correlation process (limited by the accumulator size). The data quantization (in this case m-bits X n-bits) is defined as the number of bits per symbol in each data path. Some correlators use a scheme of encoding 3 states (e.g., -1, 0, +1) onto two lines. In this article, such a scheme will be called 1.5-bit quantization. A group of L lag cells connected in series constitutes a complete correlator of lag length L.

A. VLSI Correlator Chips

TRW Corporation has been the most active in the field of custom VLSI correlator chips. They have four different products available: the TDC1004, the TDC1023, the TDC1028, and the TMC2220. The TDC1004 and TDC1023 are both 64-lag correlators with 1 X 1 (1-bit by 1-bit) data quantization. The TDC1004 outputs an analog voltage from a summing junction, whereas the TDC1023 has digital outputs and a built-in threshold register. The TDC1004 may be clocked at 15 MHz and the TDC1023 operates at 17 MHz. The TDC1028 has only 8 lags but the data quantization is 4 X 4 and full provisions are made for cascading multiple chips. Its maximum clock rate is 10 MHz. The TMC2220 is four correlators in one package, each with 32 lags and fully programmable digital outputs. It can be clocked at 20 MHz. Also in the planning stage is a new device, designated the TMC2221, which will have 128 lags and a clock rate of 20 MHz. All TRW chips have the disadvantage of not being complete correlators because they do not have accumulators on-board. This means that accumulation must be done by a computer or by external hardware.

Hughes Aircraft has developed a chip called simply the "Digital Correlator" which uses CMOS/SOS technology to make a very fast correlator. This device was designed under the VHSIC (Very High Speed Integrated Circuit) program for DARPA (Defense Advanced Research Project Agency). It is a complete correlator with 12-bit accumulators on-board. It is configured as a 128 lag device with 4 X 1 quantization and operates at a rate of 25 Megasamples/sec. It is fully cascadable with input and output SUM pins.

The Netherlands Foundation for Radio Astronomy (NFRA) has developed a VLSI correlator chip [1] which has 16 lags, 2 X 2 quantization, 22-bit accumulators and may be clocked at a rate of 55 MHz. This chip is a CMOS gate array device manufactured for NFRA by LSI Logic Corp.

RCA Corporation has a CMOS/SOS correlator chip called the TCS040 which contains two 32-lag correlators. Its outputs are analog voltages and it operates at a rate of 40 Megasamples/sec.

B. Examples of Large Correlator Systems Currently in Use

At the Arecibo Radio Observatory in Puerto Rico [2], interferometry for passive radio astronomy is performed using a correlator system which was developed for the Haystack Observatory by MIT. This machine uses conventional off-the-shelf MSI and LSI chips with ECL (Emitter Coupled Logic) used to perform the higher speed functions and F-TTL (Fast Transistor-Transistor Logic) and CMOS (Complementary MOS logic) to do the rest. This system uses 1.5 X 1.5 quantization (2-bit, 3 level quantization) and has a total of 2048 lags. It has accumulators 24 bits long and operates at a rate of 80 Megasamples/sec.

In the Communications System Research Section, a project called Goldstone Solar System Radar (GSSR) uses an in-house designed correlator [3]. Its capabilities are a 10 Megasamples/sec data rate with 4 X 1 quantization, 256 lags and accumulators 28 bits long. This data rate is used for radio astronomy and investigations of Saturn's rings. When the correlator is used for radar astronomy, the data rate is limited to 2.5 Megasamples/sec. The design is based primarily on the TRW TMC1023 chip.

The Very Large Array (VLA) in New Mexico consists of 27 antenna dishes spread over distances of up to 22 miles across the desert. Because of the large number of sources, a very large correlator system is needed [4]. The correlators are configured in arrays of 27 X 27 = 729 correlators and 16 different arrays required to perform differing types of correlation. Thus a total of 27 X 27 X 16 = 11,664 individual correlators are required. Each of these operates at a rate of 100 Megasamples/sec and uses recirculation to achieve the equivalent of 32 lags. The data is quantized 2 X 1.5 and results are summed and stored 24 bits long, as required for their fixed 52 millisecond integrate time. They have no plans for a new correlator system in the near future.

Caltech and JPL jointly operate a correlator system called the Very Long Baseline Interferometry (VLBI) Block I correlator. It has been in existence for several years and was fabri-

cated using medium-scale TTL chips. It has a total of 16 lags, data quantization of 1 X 1, accumulators 32 bits long, and correlates at a rate of 500 kilobits/sec. It is used to integrate the signals for periods ranging from 0.2 sec to 20 sec.

III. Planned or Projected Correlator Systems

Interviews were conducted with several parties who have an interest in new correlator systems. Personal visits were used where possible to learn about different types of systems under development and others merely proposed at this time. Table 3 gives a summary of the results of this survey. All of the referenced systems are either in the planning, design, or construction phase. They represent the current thinking about what can be built using the best available and most economical methods from today's technology.

The Arecibo Observatory in Puerto Rico also uses correlators to do planetary radar astronomy [2]. Their current equipment is somewhat old and they are planning to upgrade to a more modern correlator system. Jon Hagen, head of the Electronics Department at Arecibo, says that they would require a correlator with a sample rate of 1 to 4 Megasamples/sec with a lag length of 256 or 512 lags. The correlated pattern is 4095 bits long and they desire 4 X 1.5 quantization. This suggests an accumulator 16 bits long. Such a correlator is only in the planning stage at present.

In the Tracking Systems and Applications Section at JPL, there is interest in developing a system for spacecraft angular position determination using cross-correlation to perform real-time connected element interferometry. (A similar technique for spacecraft navigation was described by J. B. Thomas in JPL Internal Document, Engineering Memorandum 335-26, Jet Propulsion Laboratory, Pasadena, California, November 11, 1986.) Chad Edwards, a scientist in this section, describes the requirement as a single correlator operating at a rate of 200 Megasamples/sec using 2 X 2 quantization. Sixty-four lags would be required with each lag having a 26-bit accumulator in order to provide a 0.1 sec integrate time. These requirements are not firm at this time but represent an estimate of the needed performance.

In the Communications Systems Research Section, radar astronomer Ray Jurgens heads a group which performs planetary radar astronomy using the correlator system described in Section II. Future plans call for upgrading to a higher performance correlator system with a 50 Megasample/sec data rate, 4 X 1 data quantization, lag lengths up to 4096 bits and accumulators 28 bits long.

In the Space Physics and Astrophysics Section, radio astronomer Tom Kuiper performs astronomy using the DSN antennas. He describes a potentially useful correlator system as follows: Two correlators would be required, each operating at a 25 Megahertz bandwidth with 2 X 2 quantization and 256 to 1024 lags. The correlators should be able to accumulate for 5 to 10 minutes, which implies 40-bit accumulators. This system is a proposal only and is not currently funded.

The Owens Valley Radio Observatory (OVRO) is designing a new millimeter wave interferometer that will use high performance correlators. According to Martin Ewing at Caltech, a total of 15 correlators will be needed to handle the 15 baselines between the six 10-meter dishes being installed at the observatory. A data rate of 250 Megasamples/sec will be needed and the data will be quantized 2 X 2. Each correlator will require 512 lags and accumulators 24 bits long. This system is in the early design phase at present.

In the Observational Systems Division, plans are underway to implement an advanced radio astronomy instrument using heterodyne radiometry. Herb Pickett, an instrumentation scientist on this project, describes a system consisting of a 20-meter orbiting dish with surfaces figured to better than one micron. The plans are to cover a multi-gigahertz bandwidth using analog filters. These are expensive, high-precision filters which break the signal into several hundred bands. These bands must then be autocorrelated in order to obtain the noise autocorrelation function. The individual correlators must then operate at a rate of 65 Megasamples/sec with a 2 X 2 bit quantization. A total of 500 lags will be required for each correlator with accumulators 26 bits long. Since this is a space application, speed-power product is of prime importance and CMOS devices are the logical choice. This project is currently in the planning stage.

The DSN Data Systems Section has need for a correlator for a project called the C-band Uplink. John Smith, a group supervisor in this section, says that this correlator will need to operate at a rate of 2.4 Megasamples/sec and contain 4096 lags with accumulators 24 bits long. The data may be quantized either 1 X 1 or 1 X 4. This project is in the early design stage.

The DSN Data Systems Section also has a requirement for a correlator to perform PN (pseudo-noise) ranging (J. R. Smith, "Capabilities of the Proposed DSN Correlator Chip," JPL Internal Document IOM-3680-86-364/0, Jet Propulsion Laboratory, Pasadena, California, December 8, 1986). The correlator for this application will be required to operate at a rate of 2 to 8 Megasamples/sec with several short lag-length correlators operating in concert, the longest of which is 23 lags long. The data will be quantized 16 X 1 and accumulators 36 bits long will be needed to allow integration for several

hours at a time. This project is currently in the design phase, with a custom VLSI chip included in the plans.

In the Tracking Systems and Applications Section, Brooks Thomas is designing a high accuracy receiver for the Global Positioning Satellite (GPS) system. His requirements are for a data rate of 15 Megasamples/sec with 1.5-bit quantization. The accumulator needs to be at least 20 bits long. Each receiver will need 3 channels of correlation for each of 8 satellites, thus a total of 24 correlators. Gallium arsenide technology is being considered for this application. Work is presently in the design stage.

The Very Long Baseline Array (VLBA) is a planned series of ten 25-meter radio dishes to be located on U.S. territory from the Virgin Islands to Hawaii [6]. In addition, there are plans to link up to 10 non-VLBA antennas into an array for certain applications, making a total of 20 sources. According to John Romney of the National Radio Astronomy Observatory (NRAO), their approach to this problem is somewhat different than others in that they will perform a Fourier transform on the received signals before correlating them in pairs. First, a 2047-point transform is performed on each signal, then pairs of signals are correlated by performing a single-point multiplication of two 8-bit or 9-bit floating point numbers. The result will then be added to an accumulator of length 35 to 40 bits and accumulated for 10 seconds before dumping to the computer. This method is called the F/X method, where F represents Fourier and X represents correlation, suggesting that a Fourier transform is taken first, then correlation is performed. The data rate required will be about 32 Megasamples/sec and a total of $N(N+1)/2$ baselines will be processed. Since the VLBA needs to process signals from a maximum of $N=20$ antenna sources, processing must be provided for a total of 210 baselines. This system is currently in design and fabrication.

In the radio astronomy group at Caltech, Martin Ewing is supervising the design and construction of the Block II correlator for VLBI (Very Long Baseline Interferometry) applications. The project will consist of 168 correlators, each of which operates at up to 8 Megasamples/sec with a 1 X 1 quantization and 8 complex lags with 26-bit accumulators. This system is under construction at present and uses gate-array technology and large wire-wrap boards holding nearly 1000 chips each.

IV. VLSI Correlator Developments in the Communications Research Section

Three VLSI correlator chip projects were undertaken in this organization in the past two years which used the same sub-cells and were intended as dedicated high-speed correlators. These are called SMLCOR, BIGCOR, and RACOR. In addition, a programmable correlator/filter chip has been designed which can be externally reconfigured.

SMLCOR [5] was a proof-of-concept chip to establish that the architecture was valid and allow the design to be extended to a larger scale device. SMLCOR has 4 lags, 4-bit accumulators and 1.5 X 1.5 bit quantization. It was fabricated using NMOS technology and 4 micron feature size. It operated successfully at speeds up to 6 MHz.

BIGCOR uses an architecture based on SMLCOR but is scaled up to a much larger device of 60,000 transistors. It has 32 complex lags for a total of 64 accumulators, each with 25 bits. It uses 1.5 X 1.5 quantization but has four data paths to provide for the two real data streams and the real and imaginary parts of a phase rotator vector. A block diagram of the BIGCOR architecture is shown in Fig. 2 and the details of the correlation circuit for each lag are shown in Fig. 3. Each lag has three multipliers and the 25-bit accumulator contains one "overflow" bit which remains set until the end of a correlation cycle when it is cleared by the unload process. Both BIGCOR and SMLCOR use separate correlate and dump cycles so that correlation must be interrupted briefly while the accumulator totals are dumped out. BIGCOR was fabricated using NMOS technology and 3 micron feature size. It operates at frequencies of up to 4 MHz. Further refinements and better fabrication quality are expected to push this rate up to 10 MHz.

A chip designated RACOR (for RAdar CORrelator) has been designed using an architecture similar to BIGCOR but with 4 X 1 quantization and 32-bit accumulators (C. R. Lahmeyer, "Proposal for a VLSI Correlator for Planetary Radar," JPL Internal Document IOM 331-86.3-380, Jet Propulsion Laboratory, Pasadena, California, December 18, 1986). It was originally proposed as a VLSI design to support planetary radar observations, but may have wider application as well. It will also use NMOS technology and 3 micron feature size and has a design speed of 10 MHz. It has not yet been fabricated.

A proposed correlator system was recently described (C. R. Lahmeyer, "A Bandwidth-Multiplying Correlator," JPL Internal Document IOM 331-87.3-014, Jet Propulsion Laboratory, Pasadena, California, February 16, 1987) which incorporates the RACOR chip and a bandwidth-multiplying technique to produce a high performance correlator at a reasonable cost. Figure 4 gives a block diagram view of this design. Two banks of RACOR chips would be used so that

correlation could take place continuously without any interruption to dump the accumulator contents. Each of the two banks consists of 16 RACOR devices wired in a 4-chip by 4-chip configuration. The resulting data rate would be 80 Megasamples/sec with a 4-bit X 1-bit data quantization. The input shift register would be the only component running at 80 MHz, since the correlator chips are operating in parallel. They would need to operate at 20 MHz, however, which would necessitate their being built with high-performance CMOS technology. While this configuration has 256 lags, the number of lags is easily extendable by connecting several of these modules in series. The data quantization is also extendable by operating modules in parallel and summing the outputs with additional adder chips.

Shalhav Zohar has designed a chip which can produce the cross-correlation of sequences having a wide range of parameters ("Proposal for a Correlator/Filter Chip Based on Distributed Arithmetic," unpublished, Jet Propulsion Laboratory, Pasadena, California, February 5, 1987). Specifically, it can accommodate any system where the total number of bits involved in the computation of one correlation lag is bounded by about 1540. The correlator consists of the special NMOS chip plus a 12-bit TTL accumulator. Augmenting this setup with an external shift register produces absolute precision correlation (no roundoff error). Two extreme examples illustrate the range of possibilities: Using 64-bit input words, this system can produce 132-bit correlations based on 12-term sums at the rate of 50k correlations/sec. At the other extreme, using 1-bit words, it can produce 11-bit correlations based on 1539-term sums at the rate of 6.5M correlations/ sec.

V. Conclusions

The question now is whether any commonality exists between the various applications listed. At first glance, the similarities between the applications in Table 3 would seem to be minimal, but closer examination reveals that certain elements in common do exist between the various users. With a few exceptions, the number of lags is in the tens or hundreds. Further, most applications are for data quantizations of 1, 2, or 4 bits. The accumulator sizes required are also rather similar, centering around 25 to 35 bits. The most disparate requirement is the data rate, with values from 1 to 1000 Megasamples per second listed. Even with the great variety of speed requirements it is possible to specify an architecture which utilizes many of the common elements of several of the listed applications. The speed variation could be addressed by building the VLSI correlator chip out of appropriate VLSI technology materials to yield the required performance. For example, ECL (emitter-coupled logic) and GaAs (gallium arsenide) technologies are becoming available for custom and semi-custom chip designs of very high performance.

The bandwidth-multiplying correlator described in Section IV based on the proposed RACOR chip could be used in various combinations to satisfy approximately half of the proposed correlator applications listed in Table 3. Even higher data rates could be processed by using analog bandwidth splitting to divide the incoming signal into several streams of lower bandwidth, then performing correlation separately on each band using separate correlators. This architecture could yield reasonably low-cost correlator systems which could satisfy additional applications in the future.

References

[1] A. Bos, "The NFRA Correlator Chip," Netherlands Foundation for Radio Astronomy, Internal Technical Report No. 176, Dwingeloo Radio Observatory, Dwingeloo, Netherlands, August 1986.

[2] J. B. Hagen, "Communications Techniques in Radio Physics and Astronomy," *IEEE Communications Magazine*, vol. 24, no. 10, pp. 16–20, October 1986.

[3] S. S. Brokl, "Controller and Interface Module for the High-Speed Data Acquisition System Correlator/Accumulator," *TDA Progress Report 42-83*, vol. July–September 1985, pp. 113–124, Jet Propulsion Laboratory, Pasadena, CA, November 15, 1985.

[4] R. P. Escoffier, "Correlator System Observer's Manual," VLA Technical Report No. 39, National Radio Astronomy Observatory, Charlottesville, VA, October 1979.

[5] L. J. Deutsch and C. R. Lahmeyer, "A Systolic Architecture for Correlation and Accumulation of Digital Sequences," *TDA Progress Report 42-85*, vol. January–March 1986, pp. 62–68, Jet Propulsion Laboratory, Pasadena, CA, May 15, 1986.

[6] K. I. Kellerman and A. R. Thompson, "The Very Long Baseline Array," *Science*, vol. 229, no. 4709, pp. 123–130, 12 July 1985.

Table 1. Correlator chips currently available

Manufacturer	Part	Data Rate (MHz)	No. of Lags	Outputs	Accumulator Size (Bits)	Technology
TRW	TDC1004	15	64	Analog	N/A	Bipolar
TRW	TDC1023	17	64	Digital	None	Bipolar
TRW	TDC1028	10	8	Digital	None	Bipolar
TRW	TDC2220	20	128	Digital	None	CMOS
Hughes	–	25	128	Digital	12	CMOS/SOS
NFRA	–	55	16	Digital	22	CMOS
RCA	TCS040	40	64	Analog	N/A	CMOS/SOS

Table 2. Sample of correlator systems currently in use

System	Data Rate (Megasamples/sec)	Quantization (Bits)	No. of Lags	Accumulator Size (Bits)	Number of Correlators
Arecibo	80	1.5 × 1.5	2048	24	1
Goldstone Solar System Radar	10	4 × 1	256	28	1
Very Large Array (VLA)	100	2 × 1.5	32	24	11,664
Very Long Baseline Interferometry (VLBI) Block I	0.5	1 × 1	16	32	1

Table 3. Survey of planned correlator systems

Application	Cognizant Person	Data Rate (Megasamples/sec)	Quantization (Bits)	Number of Lags	Accumulator Size (Bits)	Number of Correlators	Current Status
Arecibo Radio Observatory, Puerto Rico	John Hagen	1–4	1.5 X 4	256–512	16	1	Planned
C-Band Uplink, Sec. 368	John Smith	2.4	1 X 1 or 1 X 4	4096	24	1	In Design
DSN Radio Astronomy, Sec. 328	Tom Kuiper	50	2 X 2	256–1024	40	2	Planned
GPS High Accuracy Receiver, Sec. 335	Brooks Thomas	15	1.5 X 1	8	20	24	In Design
Heterodyne Radiometry, (Radio Astronomy) Sec. 383	Herb Pickett	1000	2 X 2	200	26	1	In Design
Millimeter-Wave Interferometer Owens Valley Radio Observatory	Martin Ewing	250	2 X 2	512	24	15	Early Design
PN-Code Spacecraft Ranging, Sec. 368	John Smith	2–8	16 X 1	23	36	6	In Design
Planetary Radar Astronomy, Sec. 331	Ray Jurgens	50	4 X 1	4096	28	1	Planned
Spacecraft Navigation, Sec. 335	Chad Edwards	200	2 X 2	64	26	1	Planned
Very Large Baseline Array (VLBA)	John Romney	32	9 X 9 (Floating Point)	1	35-40	210	In Design
Very Long Baseline Interferometry (VLBI), Block 2	Martin Ewing	4–8	1 X 1	8 (Complex)	26	168	Under Construction

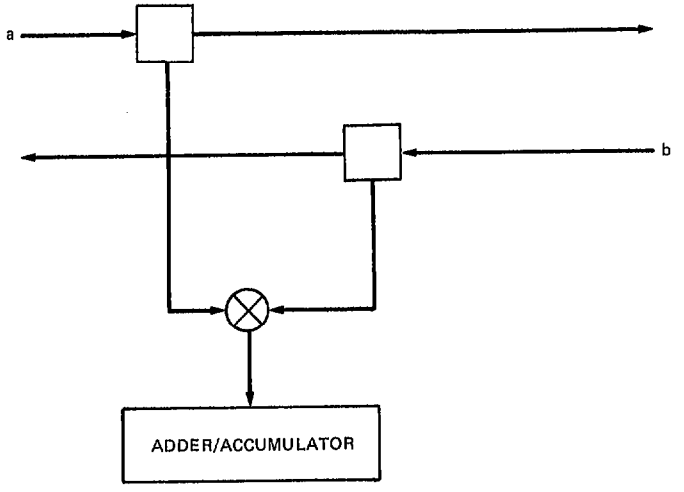

Fig. 1. Single lag cell of a typical correlator

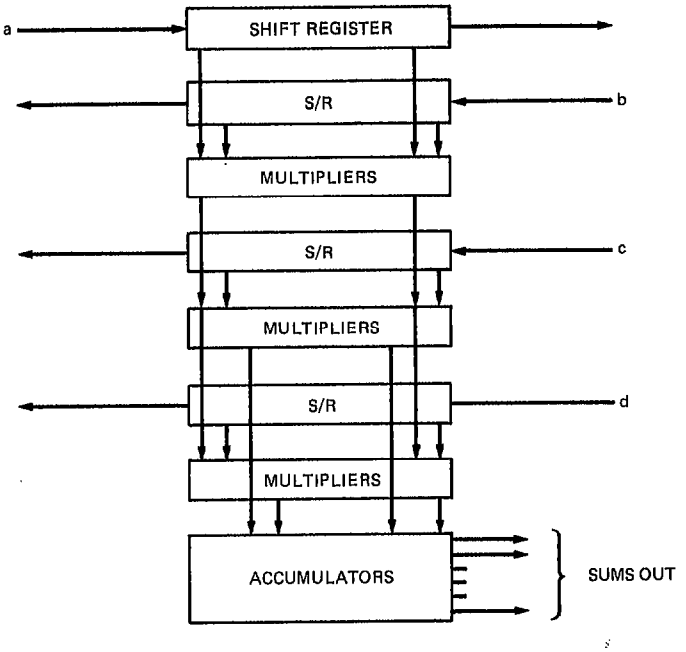

Fig. 2. BIGCOR block diagram

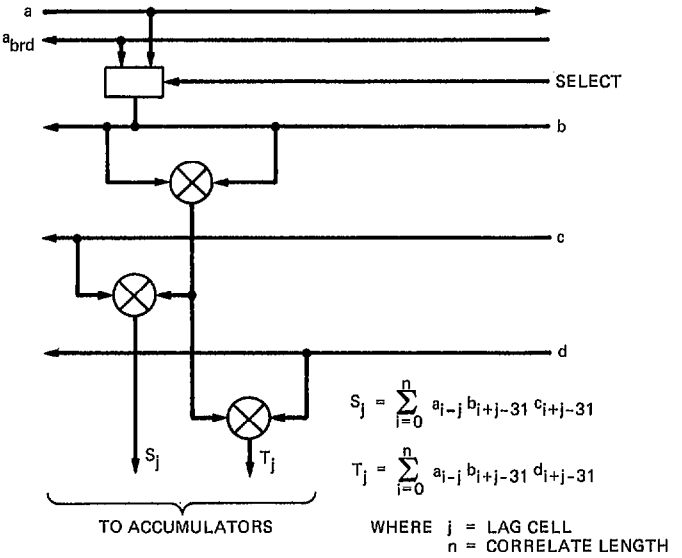

Fig. 3. Detail of BIGCOR lag cell

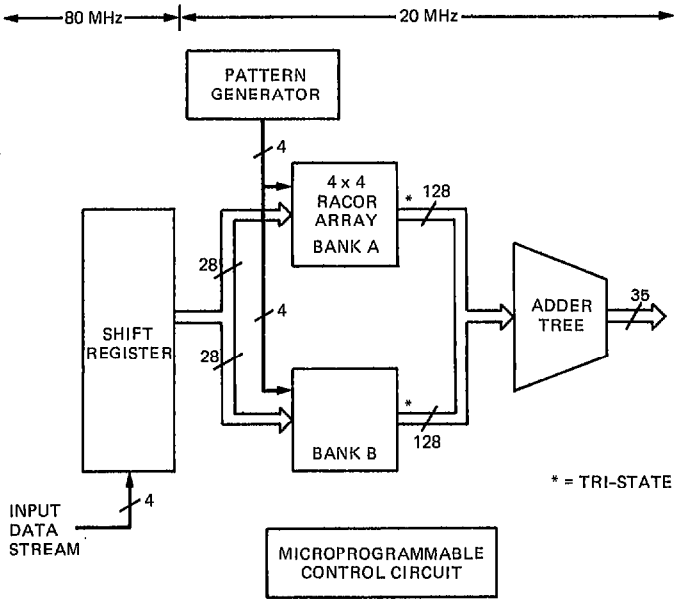

Fig. 4. Proposed VLSI radar correlator using bandwidth multiplication